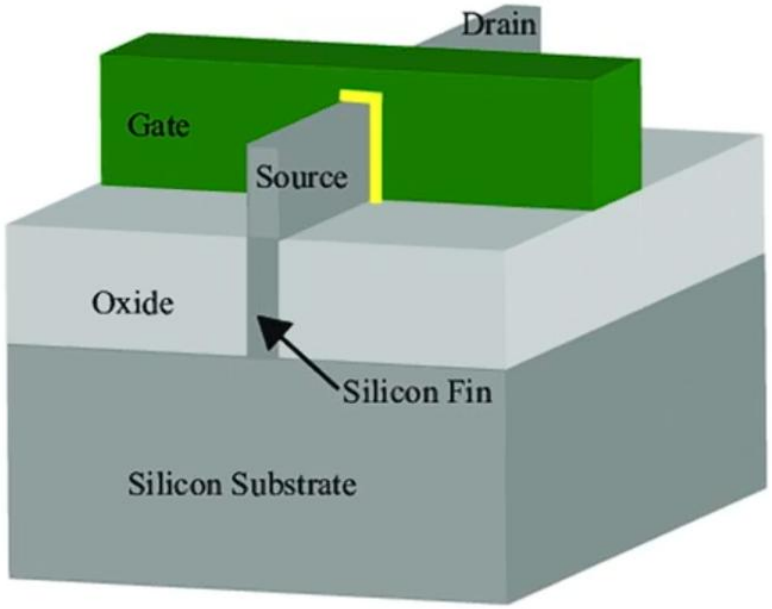
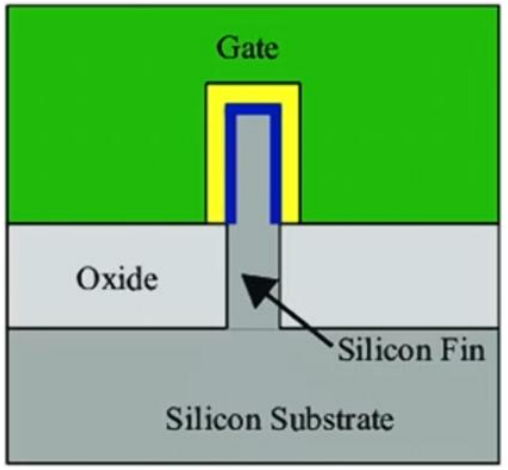
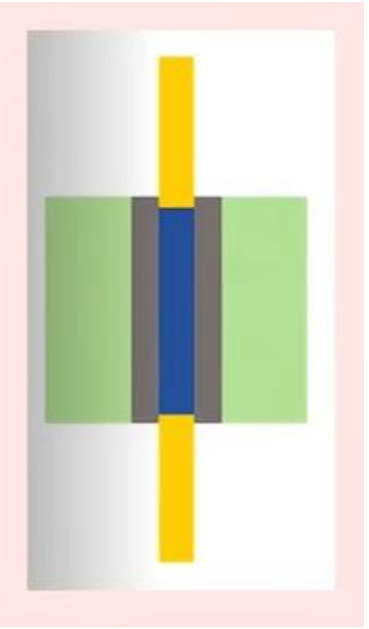
FinFET (22nm/14nm Processes ~)



(a) 3D Structure

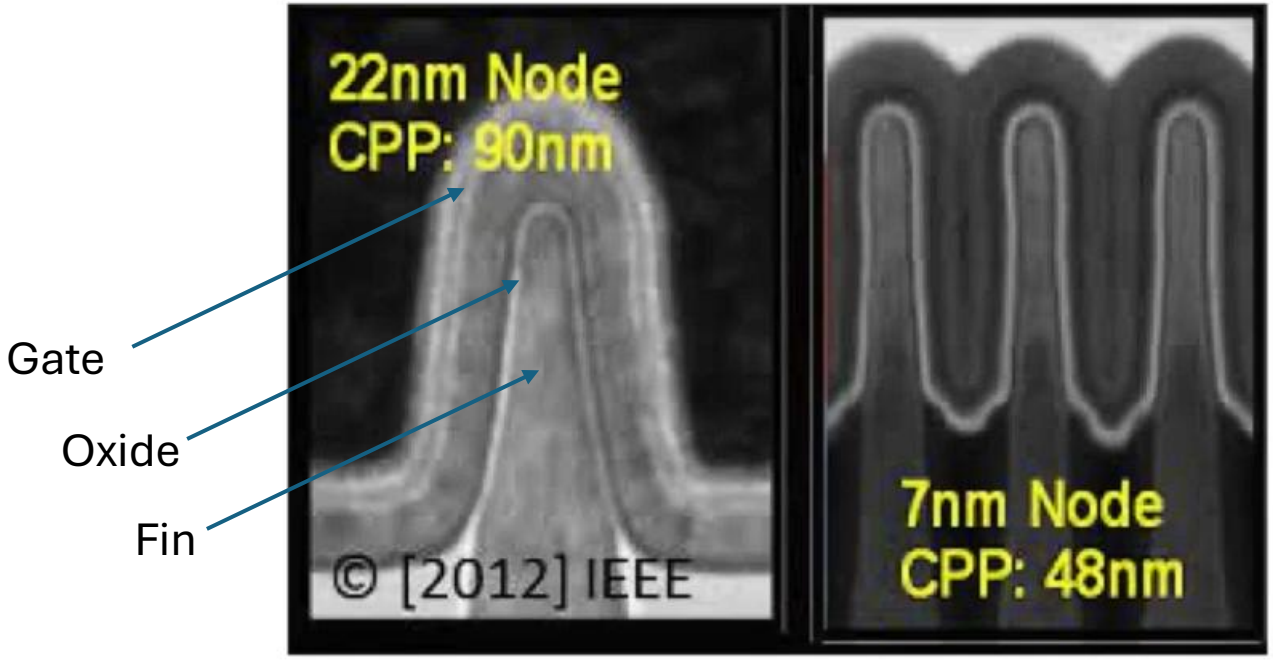


(b) Cross-sectional View

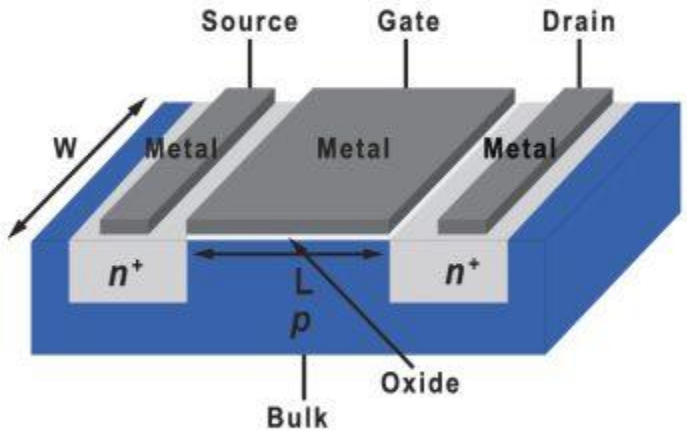


(c) Cross-section Top View

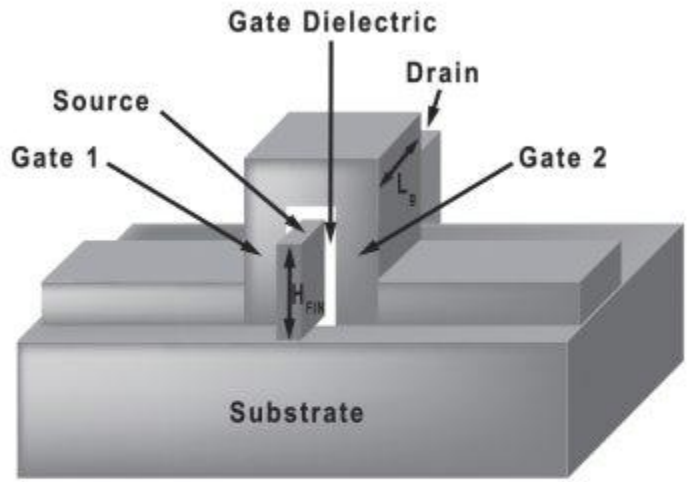
FinFET = "Double-gated" MOSFET



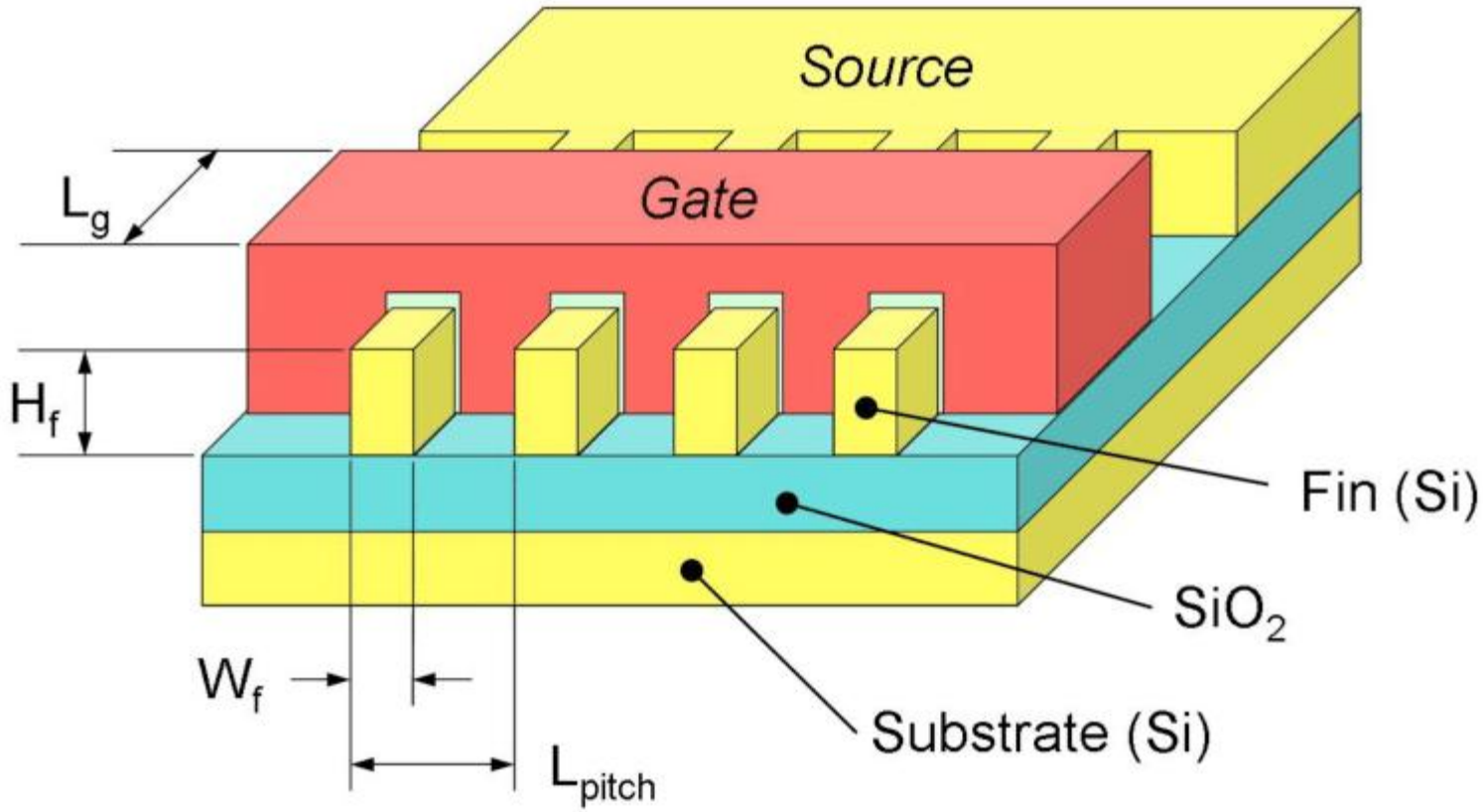
Contact Poly Pitch
90nm vs. 48nm

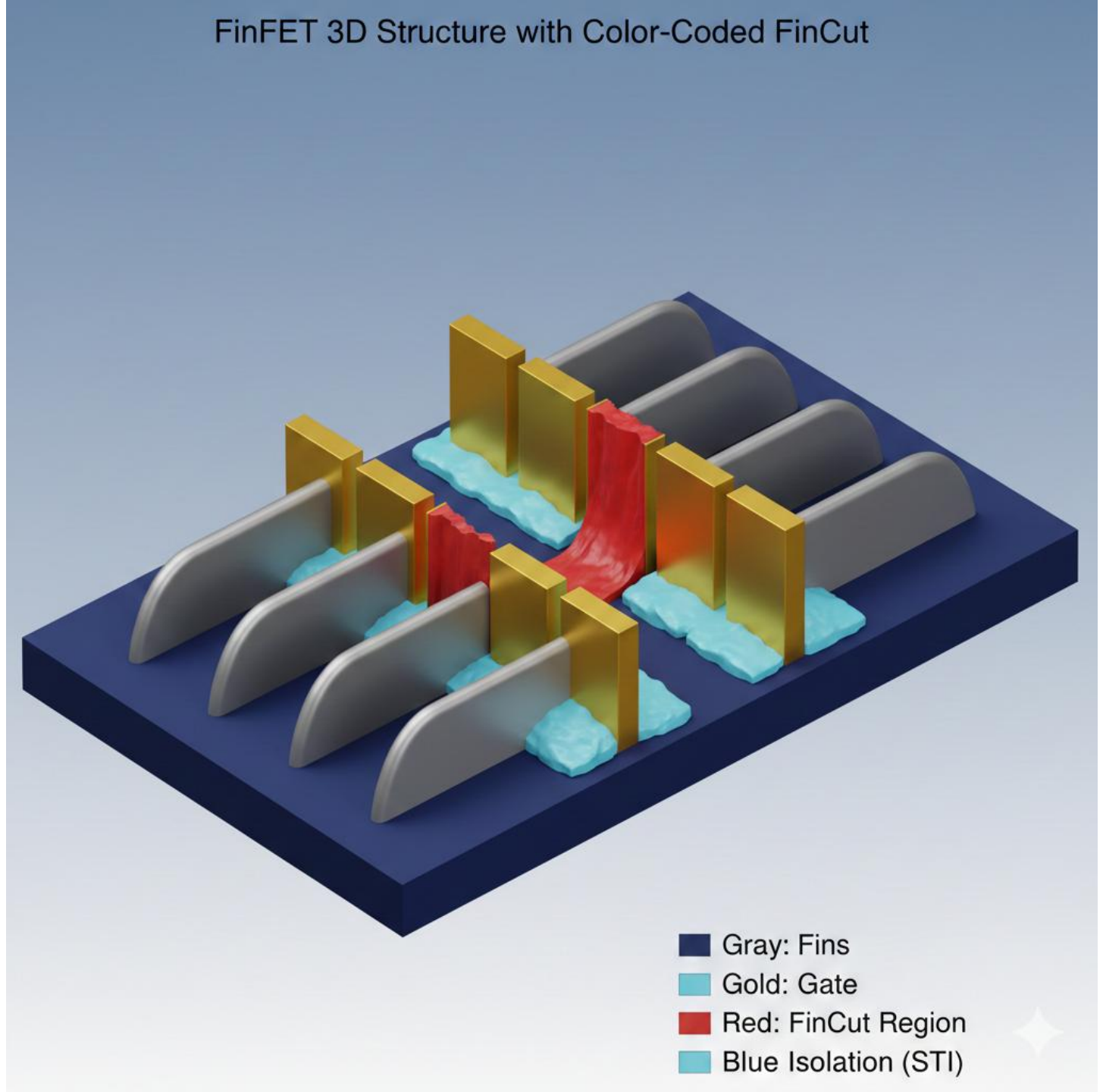


Planar MOSFET



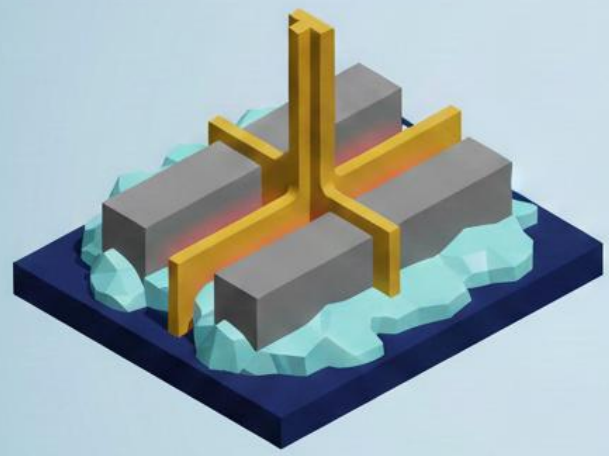
FinFET


Source
Gate
L_g
H_f
Fin (Si)
SiO_2
Substrate (Si)
W_f
L_{pitch}

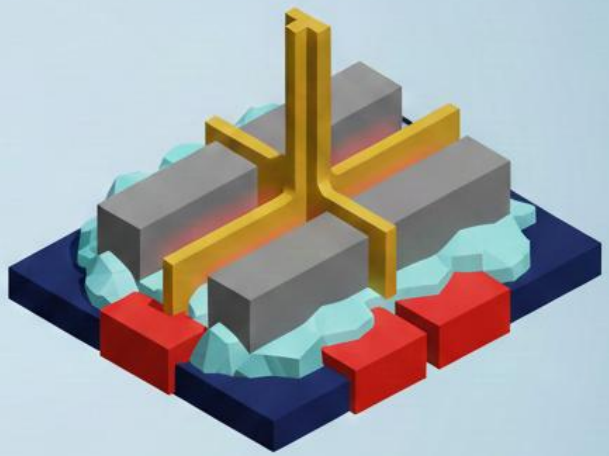

FinFET 3D Structure with Color-Coded FinCut
Gray: Fins
Gold: Gate
Red: FinCut Region
Blue Isolation (STI)

FinFET Transristor Comparison: 2-Fin vs 4-Fin with FinCut

Dual-Fin FinFET Transristor

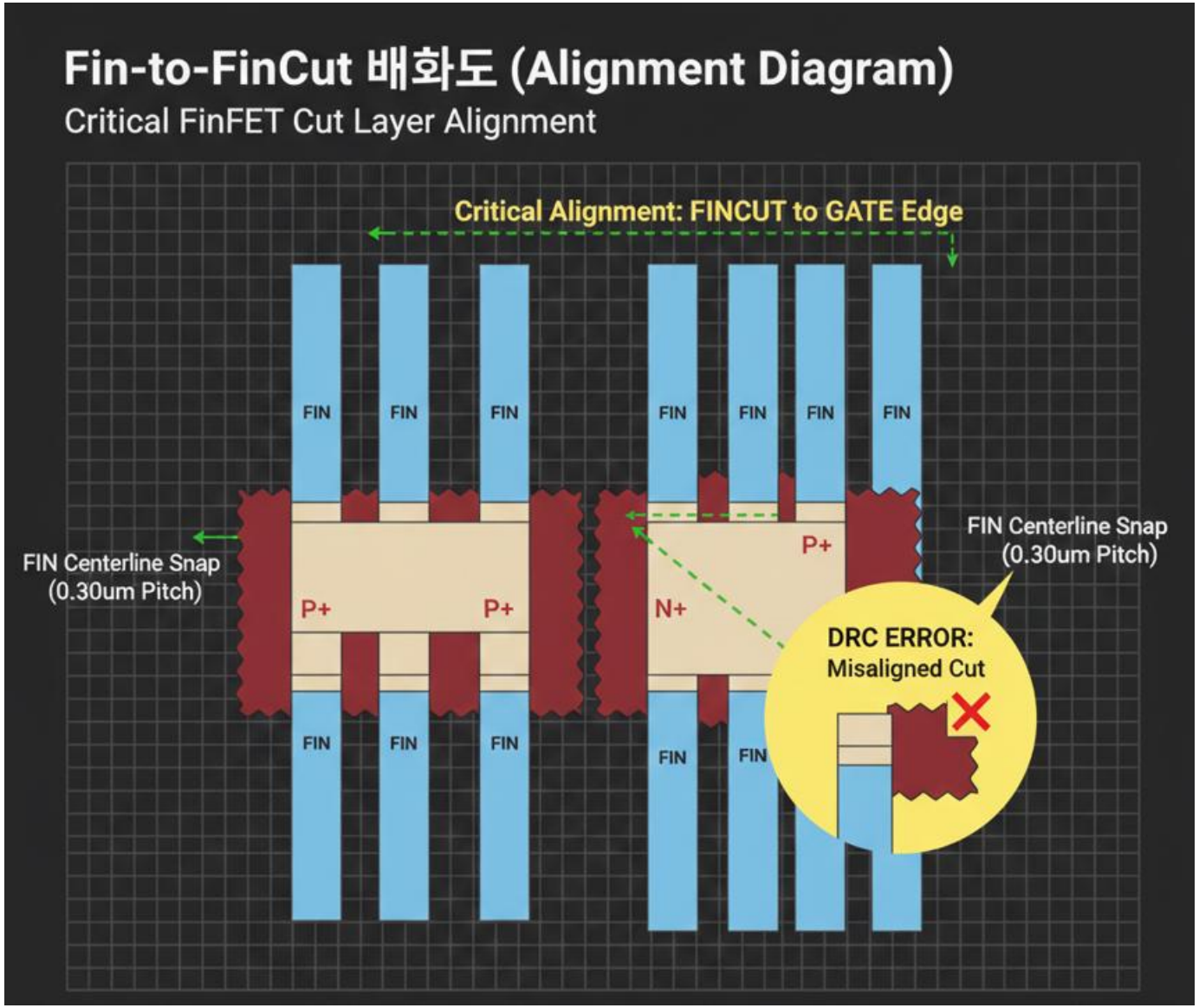


Quad-Fin FinFET Transristor



- Gray: Fins
- Gold: Gate
- Red: Active Channel Region
- Blue: Shallow Trench Istolation (STI)
- Gubstrate:
- Substrate

Note: A 4-fin transistor has approximatel twice drive current (and tus is functionally 'larger 'larger") than a due increased channel width.


Fin-to-FinCut 배화도 (Alignment Diagram)
Critical FinFET Cut Layer Alignment
Critical Alignment: FINCUT to GATE Edge
FIN
FIN
FIN
FIN
FIN
FIN
FIN
FIN Centerline Snap
(0.30um Pitch)
P+
P+
P+
N+
FIN Centerline Snap
(0.30um Pitch)
DRC ERROR:
Misaligned Cut
FIN
FIN
FIN
FIN
FIN

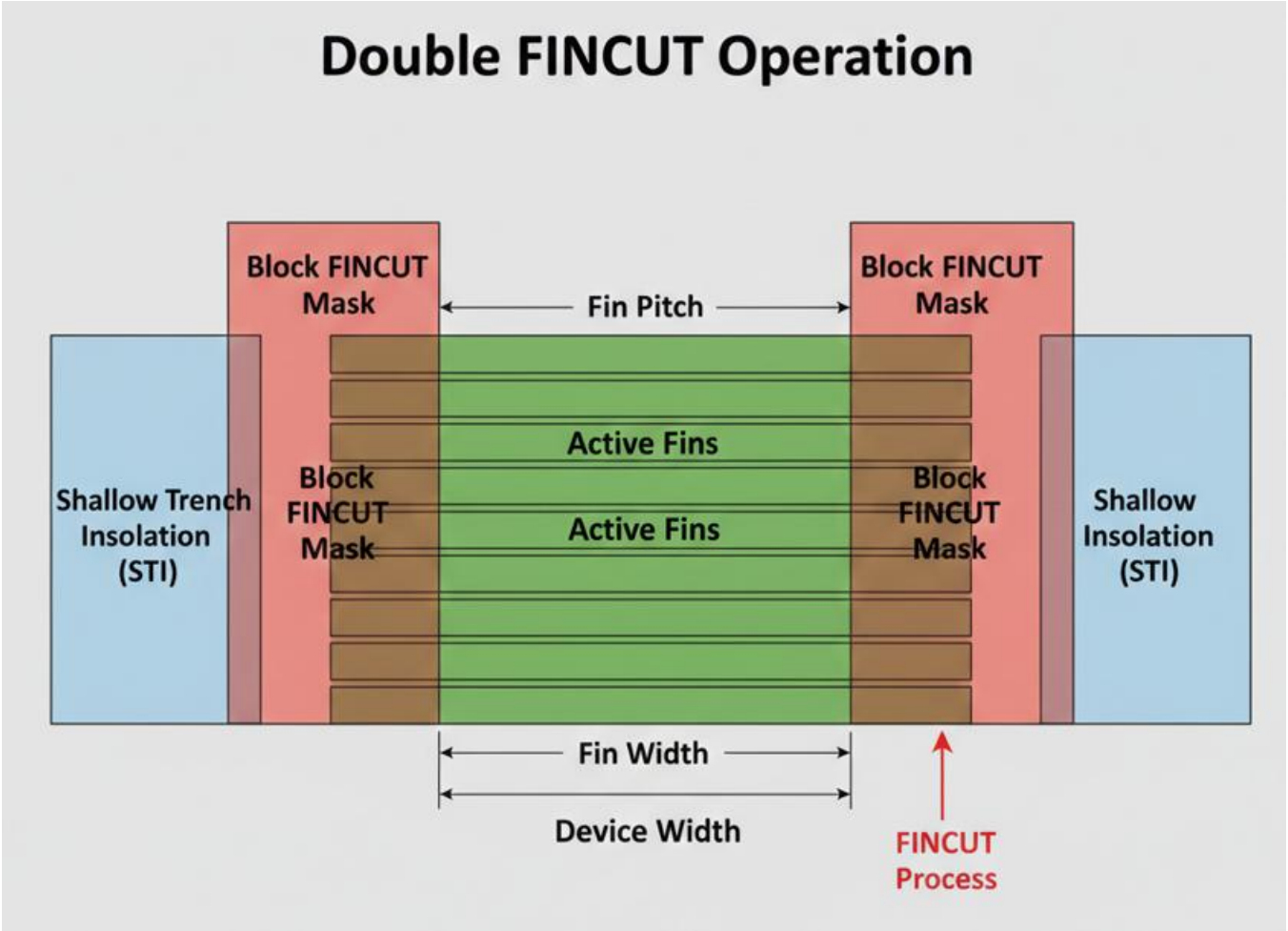
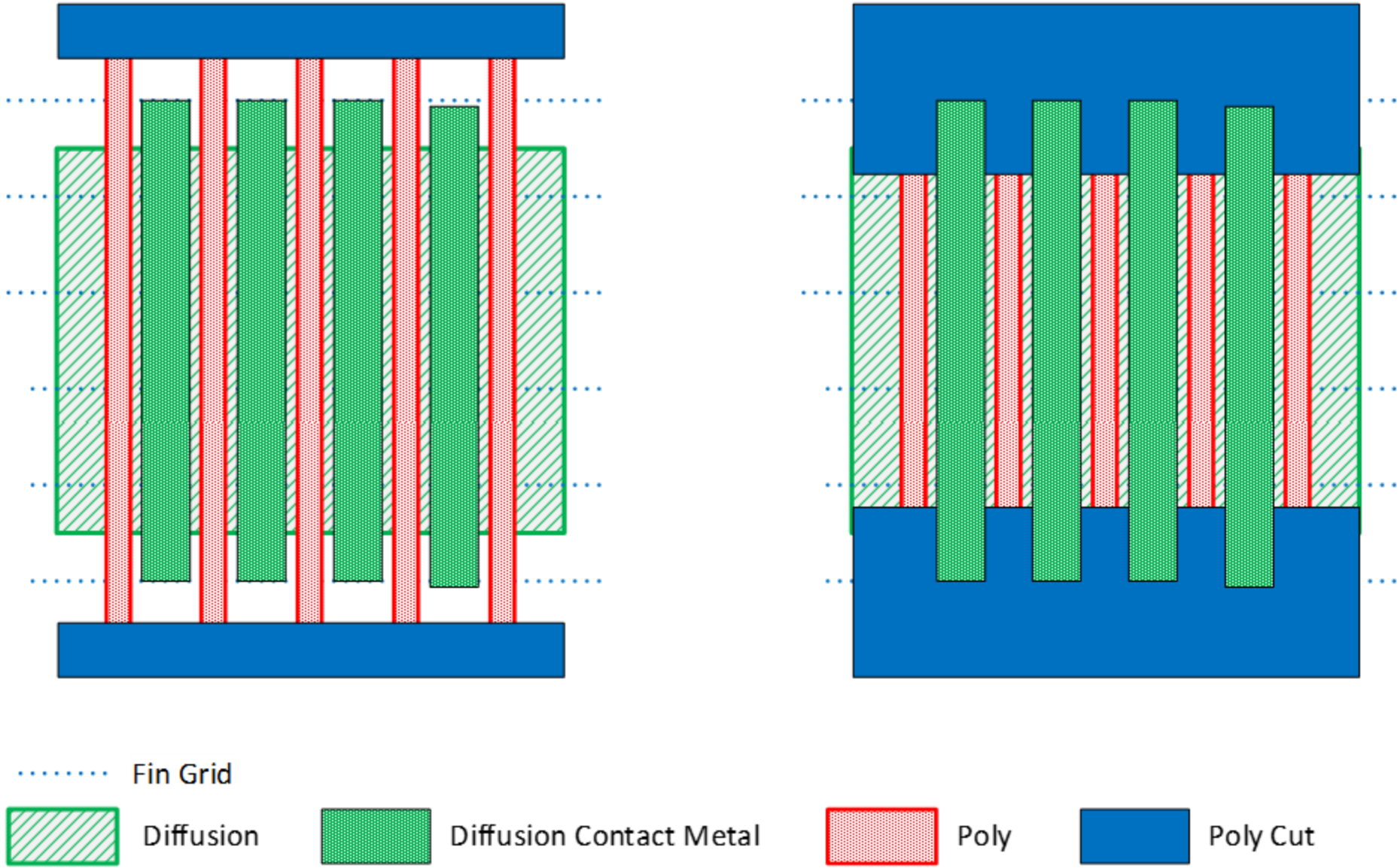
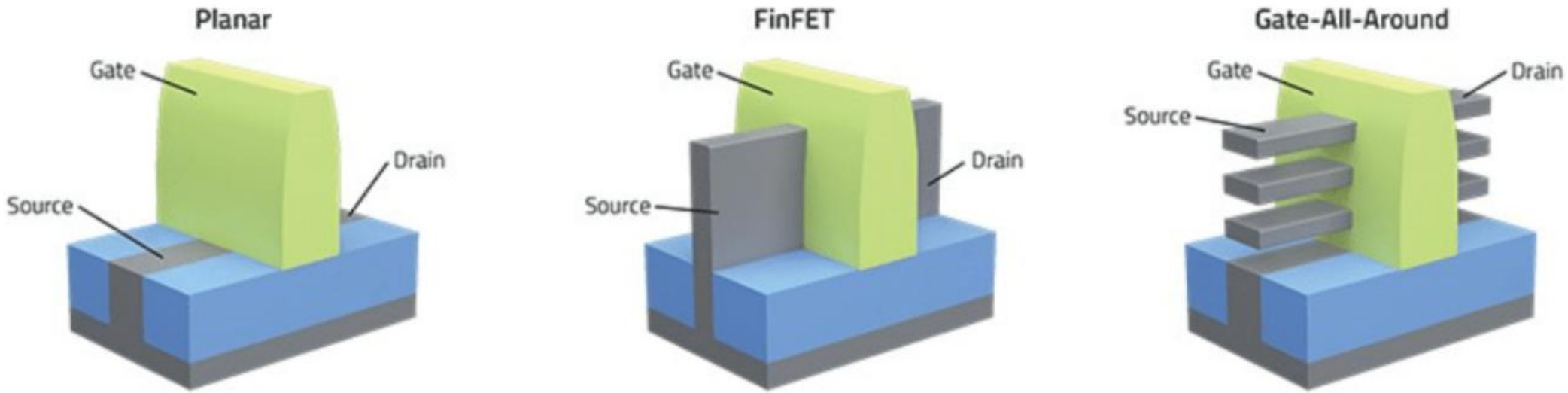

Double FINCUT Operation
Block FINCUT Mask
Fin Pitch
Block FINCUT Mask
Shallow Trench Insolation (STI)
Block FINCUT Mask
Active Fins
Active Fins
Block FINCUT Mask
Shallow Insolation (STI)
Fin Width
Device Width
FINCUT Process

Figure 2. Aggressive use of cut shapes reduces parasitic gate-diffusion capacitance.




Planar
Gate
Drain
Source
FinFET
Gate
Drain
Source
Gate-All-Around
Gate
Drain
Source