```
;============================================================
; finfet_pcell.il
;
; Reference FinFET PCell (12nm-class)
; --------------------------------
; This file demonstrates FinFET PCell architecture:
; topology-driven design, technology abstraction,
; and DFM/OPC-aware constraints.
;
; NOT intended for tape-out or direct foundry use.
;============================================================

;------------------------------------------------------------
; Technology rule abstraction (PDK-dependent layer)
;------------------------------------------------------------
procedure(loadTechRules(cv)
  let((rules)
    rules = makeTable('techRules nil)

    ; Abstract technology parameters
    rules->finPitch       = 0.04
    rules->finWidth       = 0.01
    rules->finHeight      = 0.06
    rules->minGateLength  = 0.016
    rules->gatePitch      = 0.05

    rules
  )
)

;------------------------------------------------------------
; Generate discrete fin grid (NO continuous width)
;------------------------------------------------------------
procedure(generateFinGrid(nFin finPitch)
  let((fins i)
    fins = nil
    for(i 0 nFin-1
      fins = cons(i * finPitch fins)
    )
    reverse(fins)
  )
)

;------------------------------------------------------------
; DFM / OPC guard checks
;------------------------------------------------------------
procedure(checkDFMConstraints(nFin gateLength pcmMode rules)
  when(nFin < 2 && !pcmMode
    error("Single-fin devices forbidden in product mode")
  )
  when(gateLength < rules->minGateLength
    error("Gate length below technology minimum")
  )
)

;------------------------------------------------------------
; Geometry creation (simplified 2D top view)
;------------------------------------------------------------
procedure(createFinFETGeometry(cv fins gateLength rules)
  let((x)
```

```
61
62      ; Create fins
63      foreach(x fins
64        dbCreateRect(
65          cv "FIN"
66          list(
67            x:0
68            x + rules->finWidth : rules->finHeight
69          )
70        )
71      )
72
73      ; Create gate stripe
74      dbCreateRect(
75        cv "POLY"
76        list(
77          -rules->gatePitch/2 : rules->finHeight/2
78          (last(fins) + rules->finPitch)
79          : rules->finHeight/2 + gateLength
80        )
81      )
82    )
83  )
84
85  ;-------------------------------------------------------------
86  ; Top-level PCell definition
87  ;-------------------------------------------------------------
88  pcDefinePCell(
89    list(ddGetObj("ReferenceLib") "finfet_pcell" "layout")
90
91    (
92      (deviceType "NMOS")
93      (nFin 3)
94      (gateLength 0.016)
95      (pcmMode nil)
96    )
97
98    let((cv rules fins)
99
100     cv = pcCellView
101     rules = loadTechRules(cv)
102
103     checkDFMConstraints(nFin gateLength pcmMode rules)
104     fins = generateFinGrid(nFin rules->finPitch)
105
106     createFinFETGeometry(cv fins gateLength rules)
107   )
108 )
109
```