Master ERC Whitepaper – Practical Explanation with Calibre Pseudo-Code

Introduction

Electrical Rule Checking (ERC) complements DRC and LVS by focusing on electrical correctness, voltage intent, and reliability risks. This whitepaper combines practical ERC concepts with Calibre-style pseudo-code examples, reflecting how ERC is used in real foundry, automotive, and mixed-signal IC projects.

1. Practical ERC Checks (Design-Level)

Floating Gate / Floating Net

Detects MOS gates or nets that are not driven. Floating gates can cause unpredictable behavior, especially in analog, sensor, and automotive ICs.

Code Example:

```
ERC FLOATING_GATE
  DEVICE MOS
  TERMINAL GATE
  CONDITION NOT CONNECTED
END
```

VDD–VSS Short

Detects direct or indirect shorts between power and ground that may not be caught by LVS alone.

Code Example:

```
ERC POWER_SHORT
  NET VDD
  NET VSS
  CONDITION SHORT
END
```

Multiple Driver on a Net

Identifies nets driven by multiple outputs, preventing contention and reliability issues.

Code Example:

```
ERC MULTI_DRIVER
  NETTYPE SIGNAL
  CONDITION MULTIPLE_OUTPUT
END
```

Well Tie and Bulk Connection

Ensures proper NWELL/PWELL and bulk connections to prevent latch-up and leakage issues.

Code Example:

```
ERC NWELL_TIE
  WELL NWELL
  REQUIRED NET VDD
END

ERC PWELL_TIE
  WELL PWELL
  REQUIRED NET VSS
END
```

2. Foundry-Style and Safety-Oriented ERC

Voltage Domain Crossing

Ensures proper level shifters between voltage domains to prevent gate-oxide stress and long-term reliability failures.

Code Example:

```
ERC LEVEL_SHIFTER_MISSING
  FROM_DOMAIN VDD_CORE
  TO_DOMAIN VDD_IO
  CONDITION NO_LEVEL_SHIFTER
END
```

Over-Voltage Device Protection

Prevents misuse of low-voltage devices in high-voltage domains.

Code Example:

```
ERC HV_MISUSE
  DEVICE LV_MOS
```

```
  NET VOLTAGE > LV_MAX
END
```

Power Sequencing and Back-Powering

Detects unsafe power-up sequences that may create unintended current paths, especially critical for automotive ECUs.

Code Example:

```
ERC BACK_POWERING
  FROM_DOMAIN VDD_IO
  TO_DOMAIN VDD_CORE
  CONDITION CORE_OFF_IO_ON
END
```

Safety-Critical Signal Integrity

Ensures that safety-related signals are never floating or multiply driven.

Code Example:

```
ERC SAFETY_SIGNAL
  NETTYPE SAFETY
  CONDITION FLOATING OR MULTI_DRIVER
END
```

ESD Protection Path Verification

Verifies that all IO pads have valid ESD discharge paths.

Code Example:

```
ERC ESD_PATH
  NET PAD
  CONDITION NO_ESD_DEVICE
END
```

Conclusion

Effective ERC is not a checkbox exercise but a method of encoding design intent, voltage awareness, and safety requirements into verification flows. Combining clear explanations with rule pseudo-code improves communication between designers, verification engineers, and foundries, and significantly reduces late-stage failures.