PERC ESD Topology Checks

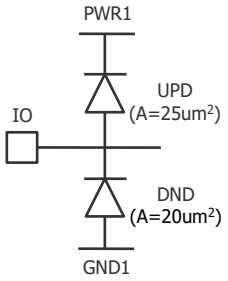
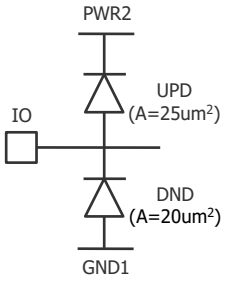
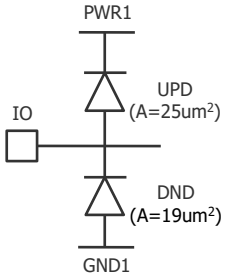
January 10, 2026

Techn Notes Park

IO Rules and Pass/Fail case

IO1 rule (ESD up/down diode on IO pad)

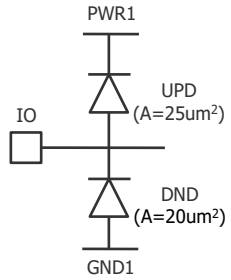
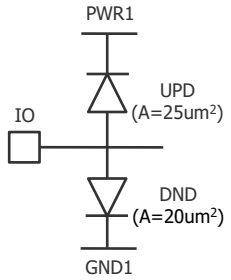
- ESD up diode and ESD down diode should exist on the IO pad
- And total area of ESD up/down diode must be 25μm²/20μm² or above

Case	Pass	Fail: No up diode	Fail: wrong prop. of down diode
Schematic			
Error message	-	ESD up diode should exist on the IO pad. But there is no UPD type diode between IO pad(anode) and PWR1 net(cathode).	Total area of ESD down diode should be 20um2 or above. But total area of ESD down diode is 19um2.

IO Rules and Pass/Fail case (Cont.)

IO1A rule (Connection of ESD up/down diode on IO pad)

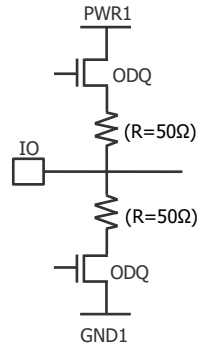
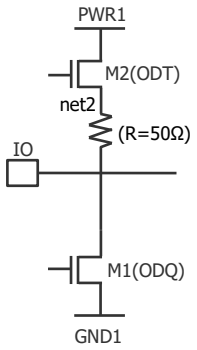
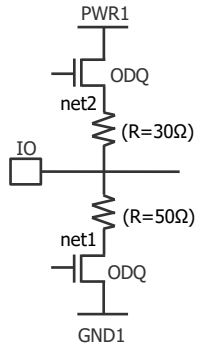
-When UPD type diode is connected to IO pad, anode must be connected to IO pad and cathode must be connected to PWR1 net
-When DND type diode is connected to IO pad, anode must be connected to GND1 net and cathode must be connected to IO pad

Case	Pass	Fail: wrong connection of down diode
Schematic		
Error message	-	When DND type diode is connected to IO pad, anode should be connected to GND1 net and cathode should be connected to IO pad. But this DND type diode is not connected as above

IO Rules and Pass/Fail case (Cont.)

IO2 rule (Resistor between IO pad and drain of ODT Tr.)

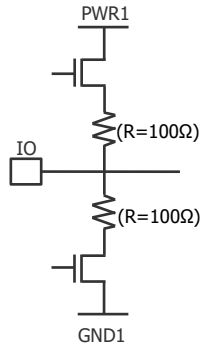
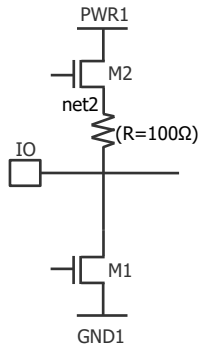
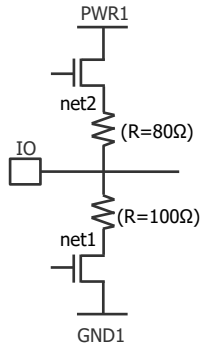
— If drain of ODT Tr. is connected to IO pad, there must be resistor between the drain and IO pad
— And total resistance of the resistors must be 50Ω or above

Case	Pass	Fail: No resistor	Fail: Wrong prop. of resistor
Schematic			
Error message	-	If drain of ODT tr. is connected to IO pad, there should be resistor between the drain and IO pad. But the drain is connected to IO pad without resistor. < List of Tr. connected directly > M1	Total Resistance of resistors connected between drain of ODT tr.(net2) and IO pad should be 50ohm or above. But the total resistance is 30ohm.

IO Rules and Pass/Fail case (Cont.)

IO4 rule (Resistor between IO pad and drain of not ODT Tr.)

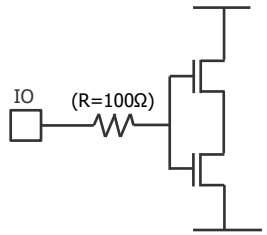
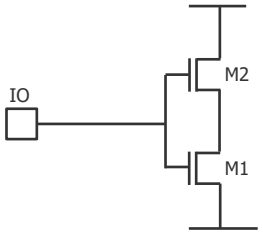
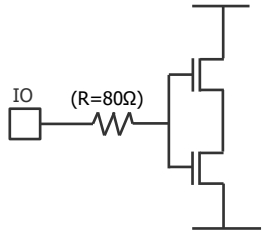
— If drain of Tr. which is not ODT Tr. is connected to IO pad, there must be resistor between the drain and IO pad
— And total resistance of the resistors must be 100Ω or above

Case	Pass	Fail: No resistor	Fail: Wrong prop. of resistor
Schematic			
Error message	-	If drain of Tr. which is not ODT Tr. is connected to IO pad, there should be resistor between the drain and IO pad. But the drain is connected to IO pad without resistor. < List of Tr. connected directly > M1	Total resistance of resistors connected between drain of tr. which is not ODT Tr. and IO pad should be 100ohm or above. But the total resistance is 80ohm.

IOBuff Rules and Pass/Fail case

IOBuff1 rule (Resistor between IO pad and IO buffer input)

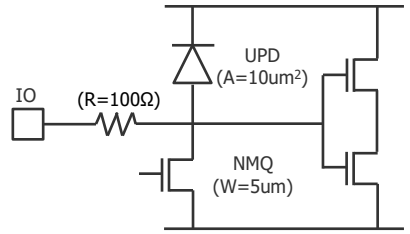
— Requires resistor between IO pad and IO buffer input
— And total resistance of the resistors must be 100Ω or above

Case	Pass	Fail: No resistor	Fail: Wrong prop. of resistor
Schematic			
Error message	-	There should be resistor between IO pad and IO buffer input. But IO buffer input is connected to IO pad without resistor. < List of Tr. connected directly > M1 M2	Total resistance of resistors connected between IO pad and IO buffer input should be 10ohm or above. But the total resistance is 80ohm.

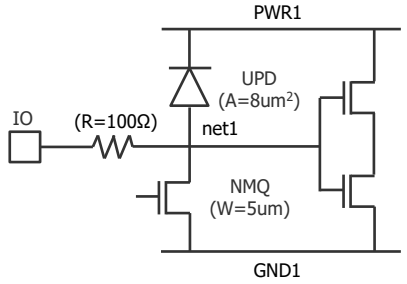
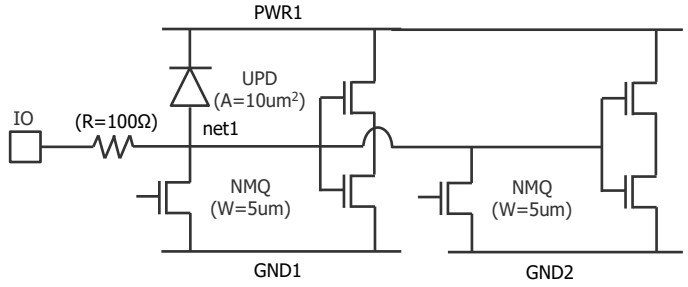
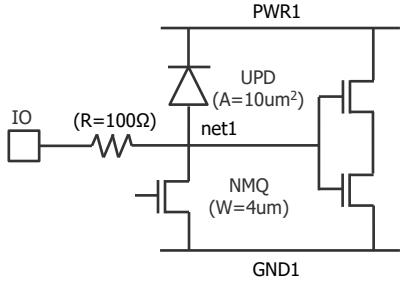
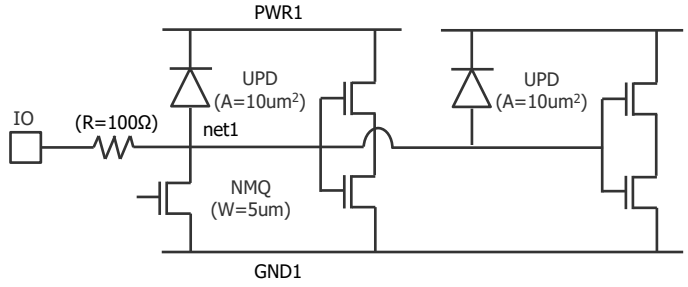
IOBuff Rules and Pass/Fail case (Cont.)

IOBuff5 rule (CDM diode and CDM Tr. on IO buffer input)

- Requires more than one CDM diode having area of 10μm² or above between IO buffer input and its Power
- Requires more than one CDM TRs having width of 5um between IO buffer input and its Ground
  (CDM TRs having same pin connection in the same cell are counted as one, and their width are summed)
- If there are more than two IO buffer connected to same IO pad and having different Grounds, each CDM diode should exist on IO buffer input
- If there are more than two IO buffer connected to same IO pad and having different Powers, each CDM Tr. should exist on IO buffer input

Case	Pass
Schematic	

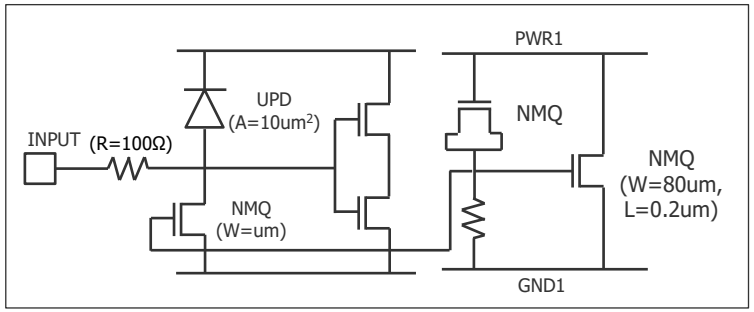
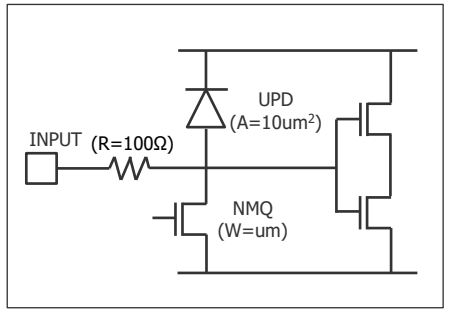
IOBuff Rules and Pass/Fail case (Cont.)

Case	Fail: No CDM diode	Fail: Shortage of CDM diode
Schematic		
Error message	There should be more than one CDM diode(UPD) having area of 10um2 or above between IO buffer input(net1) and its Power(PWR1). But there is no CDM diode having area of 10um2 or above between net1 and PWR1 net.	If there are more than two IO buffer connected to the same buffer input(net1) and having different 2 Grounds, 2 CDM diodes(UPD) should be exist between net1 and PWR1 net. But there is only 1 CDM diode between net1 and PWR1 net.
Case	Fail: No CDM Tr.	Fail: Shortage of CDM Tr.
Schematic		
Error message	There should be more than one CDM Tr.(NMQ) having width of 5um or above between IO buffer input(net1) and its Ground(GND1). But there is no CDM Tr. having width of 5um or above between net1 and GND1 net.	If there are more than two IO buffer connected to the same buffer input(net1) and having different 2 Powers, 2 CDM Tr.s(NMQ) should be exist between net1 and GND1 net. But there is only 1 CDM Tr. between net1 and GND1 net.

IOBuff Rules and Pass/Fail case (Cont.)

IOBuff6 rule (Connection of CDM Tr.s gate)

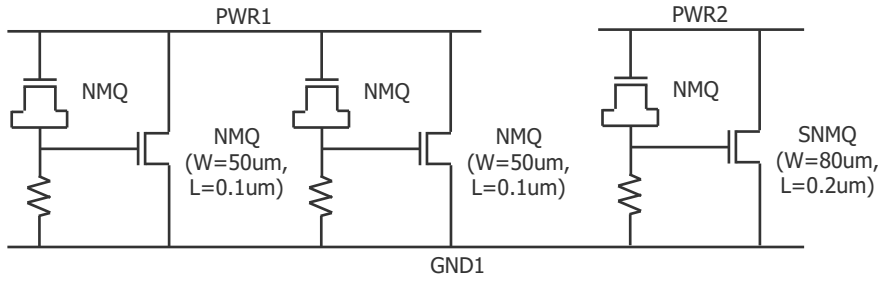
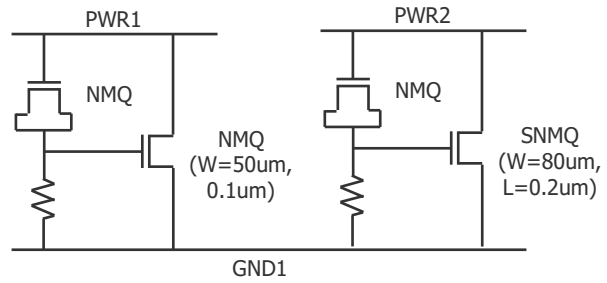
— Gate of CDM Tr. must be connected to the gate of Power clamp connected to the same Power(PWR1) and ground(GND1) of IO ESD diodes

Case	Pass	Fail: Wrong connection of CDM Tr. gate
Schematic		
Error message	-	Gate of CDM Tr. should be connected to the gate of Power clamp connected between PWR1 net and GND1 net. But this CDM Tr.'s gate is not connected to the gate of Power Clamp connected between PWR1 net and GND1 net.

Power Clamp Rules and Pass/Fail case

Power1 rule (Power Clamp(Tr + R + C) on each Power lines)

— Each Power lines should have enough Power Clamp satisfying 'Power5' rule to each ground lines
— Enough number of Power Clamp for each Power are as below
Syntax) Power name: Power Clamp count (PWR1: 2, PWR2: 1)

Case	Pass	Fail: Shortage of Power Clamp
Schematic		
Error message	-	PWR1 Power net should have more than 2 Power Clamp to each Ground nets. But there is only 1 Power Clamp between PWR1 net and GND1 net

Power Clamp Rules and Pass/Fail case (Cont.)

Power5 rule (Power Clamp)

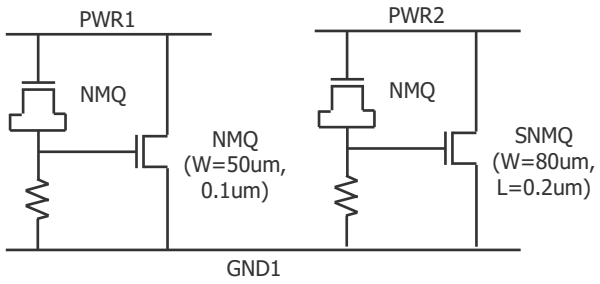
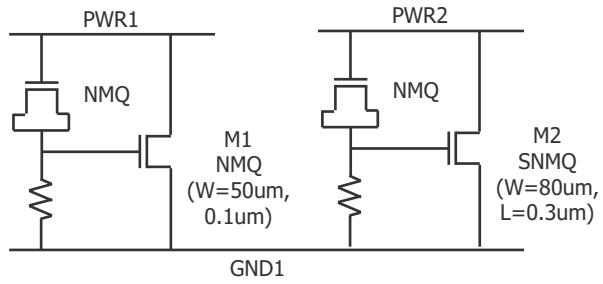
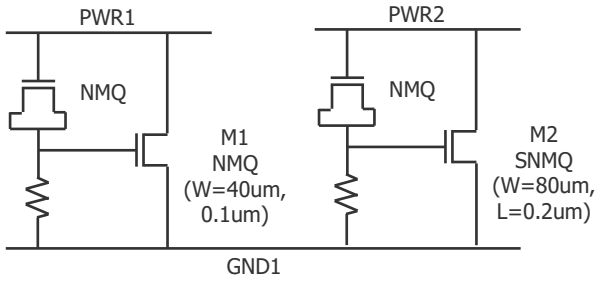
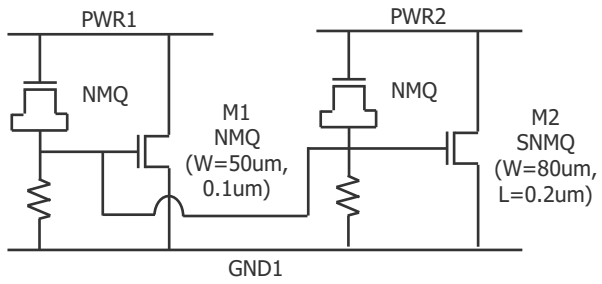
— The length of the Power Clamp TR must be the same as criteria of Power Clamp TR length

— The total width of the Power Clamp TR connected to the same gate net must be criteria of Power Clamp Tr. width or above

— Each criteria for each Powers are as below
Syntax) Power name: Power Clamp TR Subtype/Power Clamp TR Width
/Power Clamp TR length/MOS cap.
Subtype (PWR1: NMQ/50um/0.1um/NMQ, PWR2: SNMQ/80um/0.2um/NMQ)

— The gate of Power Clamp TR should not be connected to other gate of Power Clamp type TR having different Power or Ground net

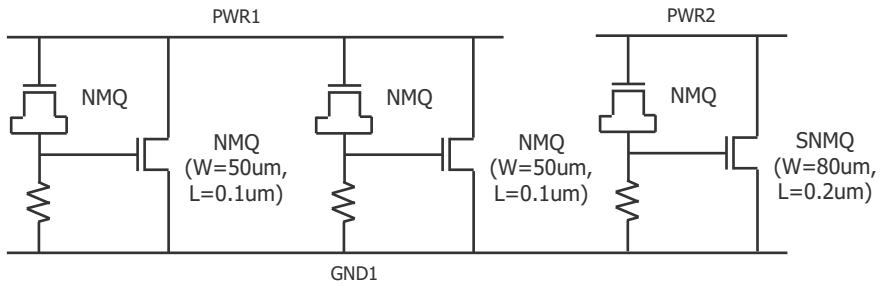
Power Clamp Rules and Pass/Fail case (Cont.)

<table>
<tr><td>Case</td><td>Pass</td><td>Fail: Wrong length of power Tr.</td></tr>
<tr><td>Schematic</td><td> 
</td><td> 
</td></tr>
<tr><td>Error message</td><td>-</td><td>The length of the Power Clamp Tr. on PWR2 net should be 0.2um.
But there is Power Clamp Tr. having wrong length.
< List of Tr. having wrong length >
M1</td></tr>
<tr><td>Case</td><td>Fail: Wrong width of power Tr.</td><td>Fail: Wrong connection</td></tr>
<tr><td>Schematic</td><td> 
</td><td> 
</td></tr>
<tr><td>Error message</td><td>The total width of the Power Clamp Tr.(NMQ) on PWR1 net connected to the same gate net should be 50um or above.
But total width is 40um.</td><td>The gate of Power Clamp Tr. should not be connected to other gate of Power Clamp type Tr. having different Power or Ground.
But on this nets, there are Power Clamp Tr.s having different Power or Ground net.
< List of Power Clamp Tr. connected together >
M1 M2</td></tr>
</table>

Power Clamp Rules and Pass/Fail case (Cont.)

PWRCLP_info (Number of Power Clamp and total width of Power TR)

— PWRCLP_info' reports the Number of Power Clamp satisfying 'POWER5' rule and total width of Power Clamp TR on each POWER net

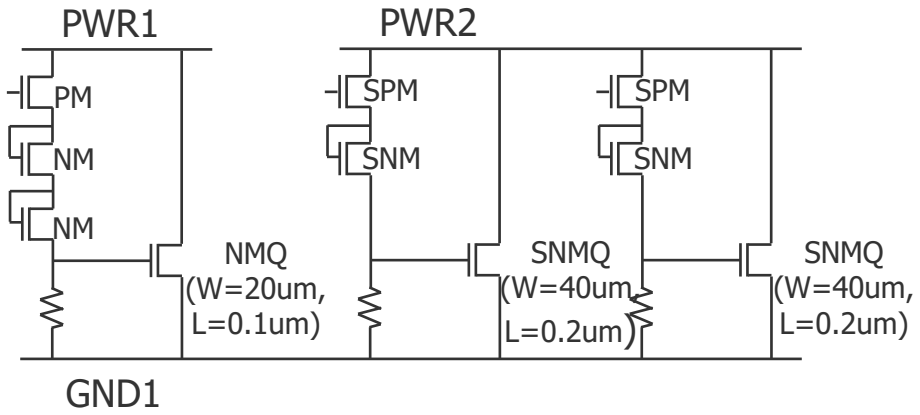
example	
Message	Between PWR1 and GND1 Number of Power Clamp: 2 Total width of Power Clamp Tr.: 100um Between PWR2 and GND1 Number of Power Clamp: 1 Total width of Power Clamp Tr.: 80um

EOS Clamp Rules

EOS rules are similar to Power Clamp rules

- But the structure of EOS clamp is different
- Each Power net has criteria as below
  - Syntax) Power name: EOS Clamp count/Total width of EOS Clamp TR
  - Example) PWR1: 1/20um, PWR2: 2/80um
- Each EOS Clamp has criteria as below
  - Syntax) Power name: EOS Clamp TR subtype/ EOS Clamp TR Length/ Mos diode subtype / Mos diode count/ Mos switch subtype
  - Example) PWR1: NMQ/0.1/20/NM/2/PM, PWR2: SNMQ/0.2/40/SNM/1/SPM

< Example schematic off EOS Clamp >



Structure of the Ruledeck

0_RuleSpec:	File for deck developers to modify the rule criteria
1_Control:	File for users to fill in the input data for running the ruledeck
2_PortSort:	Execution file that creates 'Port.info' file
3_Run:	Rule check execution file
4_view:	RVE execution file
Port.info:	File including some information for users to check before executing '3_Run'
Include:	Directory that includes PERC golden rule coding files

- Verifying Flow

Fill in '1_Control' according to the design ▪ Run '2_Port_Sort'
→ Check 'Port.info' if all information in it are ok ▪ Run '3_Run'
→ Run '4_View' and examine errors

Overview of Ruledeck (Cont.)

- **'0_RuleSpec' includes the sections to fill in …**

  — Rule criteria of rule checks as below

```
#< Variables for IO rules >
variable IO_ESD_Updio_Pwr {VDD}
variable IO_ESD_Updio_Subtype {npn}
variable IO_ESD_Updio_Area {20}

#< Variables for Power rules >
#{{PwrNet1 PwrMos_Subtype1 PwrMos_W1 PwrMos_L1 MosCap_Subtype1 PwrClp_Cnt1} … }
Variable PWRCLP_Specs {{VDD NMOSQ 200 0.1 NMOS 3} {VDD1 SNMOSQ 150 0.08 NMOS 2}}
```

- '1_Control' includes the sections to fill in …

  — Source path, source primary
  — Rule names to run (IO rule/INPUT rule/ …)
  — Port names that users want to exclude from 'LvsTopPorts'
  — Default/special Power and Ground port names
  — IO, Input and other port names needed in rule checks

Overview of Ruledeck (Cont.)

- **'Port.info' includes information of …**
  - Input netlist path/Top cell names/Selected rules to run
  - All port names and count (Which are 'LvsTopPorts' ports)
  - Power/Ground port names and count
  - IO/Input/other port names and count
  - Not defined port names and count

- Before executing '3_Run', users should check if the port names in the 'Port.info' are correctly defined

- This check is for users not to miss a port that must be checked

Overview of Ruledeck (Cont.)

Rule checks

— PreESD Check
- This rule is for pre-checking of ESD topology before main checking
  This check verifies whether there is any ports that doesn't have diode or Power MOSFET on it

— IO/INPUT rules
- Verifies whether IO/INPUT ports have proper ESD protections of them

— IoBuff/InputBuff rules
- Verifies whether IoBuff/InputBuff nets have proper ESD protections for them

— Power Clamp/EOS Clamp rules
- Verifies whether all power nets and ground nets have proper Power Clamp and EOS Clamp

— ERC rules
- Verifies whether there is nmos/pmos gate connected to power/ground nets

— Probing Pad/TSV rules
- Verifies whether Probing Pad/TSV ports have proper ESD protections for them