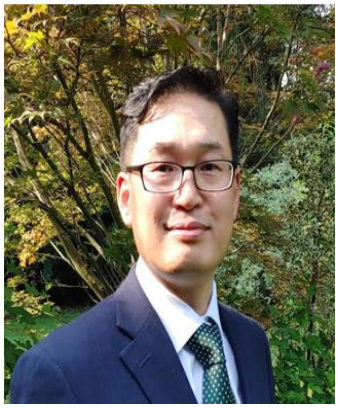
# Kyung Wook Park



Munich, Germany
EU Long-Term Residence Permit (Daueraufenthalt-EU)
English (C2) • German (B2) • Korean (Native)
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## PROFESSIONAL SUMMARY

• Senior semiconductor professional with 30 years of experience **across EMEA and APAC**, spanning **advanced IC design, EDA verification, design-to-mask preparation**, and **complex, high-value B2B engagements**.

• Proven ability to **align customer business priorities with advanced semiconductor** and **EDA application solutions**, effectively bridging design, verification, and **manufacturing readiness** for **complex, safety-critical programs**, including automotive products.

• **Commercial leadership & APAC sales** combined with **sign-off–level technical credibility**; partner to **senior management**, CAD teams, and **global foundries** to drive adoption, de-risk tape-outs, and deliver sustained revenue growth

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## KEY ACHIEVEMENTS

• **Enabled production-ready tape-outs for safety-critical automotive and advanced semiconductor products**, including Bosch's 300mm automotive chip, by leading photo-mask preparation, OPC/RET, manufacturability validation, and data integrity assurance

• **Supported PDK development and validation** for leading foundries including TSMC, Intel, GlobalFoundries, Samsung, Infineon, and ST, acting as a trusted technical and commercial advisor to ensure successful customer outcomes across Europe and APAC

• **Developed automation frameworks and verification flows** (SKILL-based PCells, TCL/SVRF/TVF scripts, standard libraries), improving verification throughput, accuracy, and customer sign-off turnaround time

• **Bridged engineering, manufacturing, and customer teams**, translating complex design, sign-off, and yield considerations into clear execution plans that reduced program risk and accelerated adoption

• Recognized with multiple company **awards**, including **SK Hynix** Key Talent Award, Outstanding Achievement Award, Best Product Award, and **GlobalFoundries** BestSupport Award

• **Authored 14 patents (2 U.S., 12 Korean)** in DRAM memory circuit design and physical design, reinforcing technical credibility in customer and executive discussions

• Drove **multi-million-euro** semiconductor sales and business development cross APAC, securing **Tier-1 customer relationships,** leading long-cycle, high-value B2B engagements

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## CORE PROFESSIONAL COMPETENCIES

• **Enterprise Sales, Go-To-Market Strategy**, Negotiation and Deal execution
• Regional Sales Leadership & Cross-Cultural Stakeholder Management
• **Customer Success & Account Enablement** (technical advisory, EMEA & APAC)

• **Semiconductor Solution Positioning** (Memory, ASIC, Analog & Mixed-Signal)
• Foundry Partnership & Ecosystem Collaboration (TSMC, Intel, GF, Samsung, ST)
• **R&D–Customer Alignment & Cross-Functional Leadership**

• **EDA / DFM / Verification Expertise** supporting customer evaluations and adoption
• Tape-Out, Full-Chip Sign-Off & Mask Data Preparation (OPC/RET, Kerf)
• **Yield, Manufacturability & Reliability Optimization** aligned with business outcomes
• Design Automation & Workflow Optimization to accelerate customer sign-off

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## PROFESSIONAL EXPERIENCE (Expert Track – Semiconductor / Manufacturing / EDA)

**Robert Bosch Semiconductor Manufacturing Dresden,** Dresden, Germany
**Expert, Design-to-Mask Preparation** | 2025.04 – 2025.10

• **Led end-to-end tape-out and photomask preparation** for a 300mm automotive semiconductor program, ensuring manufacturability, data integrity, and compliance with automotive quality standards, frame generation, multi-die placement

• **Identified and mitigated manufacturing-readiness risks** during technology transfer (TI / TSMC 45nm) by implementing **reticle**, kerf, and alignment optimizations, reducing re-spin exposure, creating alignment, overlay markers, metrology targets, CD-control features, PDM cell

• **Coordinated cross-functional stakeholders** across design, lithography, manufacturing, and mask vendors to deliver a production-ready mask set under strict schedule constraints

• Performed and **calibrated model-based OPC** for the 110 nm node, leveraging **RET strategies** in collaboration with the photolithography modeling team

***Impact***: Enabled on-time production release of a **safety-critical automotive semiconductor** by mitigating tape-out and manufacturability risks under strict quality and yield

**Siemens EDA (Electronic Design Automation, Mentor Graphics),** Munich, Germany
**Senior Customer Application Engineer (Calibre Portfolio)** | 2014.06 – 2025.03

• Served as a **trusted technical advisor** to Tier-1 semiconductor companies (Intel, Infineon GlobalFoundries, ST, Apple), supporting **strategic decisions** across verification, manufacturability, and sign-off

• Led **customer engagements end-to-end** from problem framing and solution benchmarking to **implementation, automation, and tape-out readiness in IC Physical design solutions**, directly influencing project outcomes and schedules

• Designed and deployed **custom verification & automation flows** (DRC/DFM/PERC/LVS), PDK, eliminating recurring bottlenecks and reducing late-stage design and manufacturing risk

• **Focused on IC manufacturing backend** and customer application engineering for Calibre **OPC / RET (Resolution Enhancement Technology)** in foundry environments

• Strong expertise in RET-driven lithography enablement, integrating **SRAF** (Sub-Resolution Assist Feature) engineering, Mask Data Preparation (MDP), **multi-patterning strategies**, ILT-based simulation, MPC, and verification flows to optimize **layout manufacturability**.

• **Delivered leadership-level briefings and technical workshops**, and **enablement sessions**, aligning engineering teams and decision-makers on adoption of advanced verification and manufacturability solutions

***Impact***: Drove adoption contributing to multi-year enterprise agreements of **Calibre verification and DFM solutions** across multiple Tier-1 customers, strengthening long-term strategic partnerships and accelerating customer time-to-market.

**DSP-Weuffen GmbH,** Amtzell, Germany
**Consultant Sales Engineer (Asia Market)** | 2013.02 – 2013.11

• **Led technical sales engagements** for ADAS, multi-camera, MCU, and DSP platforms across China and Korea, supporting customer evaluations and design-in decisions

• **Developed and managed Tier-1 automotive accounts** including Delphi, Mando, Hyundai Mobis, and Desay, acting as the primary technical and commercial interface

• **Delivered system-level HW/SW demonstrations** (surround-view and vision systems) and supported customer benchmarking and feasibility assessments

**Impact:** Accelerated evaluations shortening sales cycles and design-in discussions for automotive electronics platforms across **APAC** by translating system-level capabilities into customer-specific value.

**Infineon Technologies AG**, Munich, Germany
**Consultant – IC Package / PDK Engineer** | 2012.12 – 2013.09

• Developed **Calibre-based DRC rule decks** for **wire-bond BGA, TSSOP, and MQFP LF packages**, supporting standardized package verification flows

• Created **test cases and validation frameworks** to ensure rule-deck accuracy, production readiness, and proper documentation

• Coordinated **OSAT alignment** with **Amkor Technology and ASE**, ensuring consistency between design rules, package implementation, and manufacturing constraints

***Impact*:** Enabled production-ready package verification flows and smoother OSAT integration, reducing risk during package qualification and manufacturing ramp-up.

**ELMOS Semiconductor SE**, Dortmund, Germany
**Senior Sales Representative (APAC)** | 2010.01 – 2012.09

• Managed **sales operations and distributor networks** across Singapore, Korea, China**,** Japan, and Taiwan, serving as the primary interface for OEM / Tier-1 automotive customers

• Generated **€15M in revenue** for **ultrasonic parking sensor ICs** by driving customer engagement, design-in activities, and long-term account development

• Led **contract and pricing negotiations** with major customers including **Hyundai Mobis**, Panasonic, Delphi, and Alpine, balancing technical requirements with commercial objectives

• Delivered **end-to-end technical and commercial design-in support** for automotive ASIC projects spanning sensing, power management, motor control, and in-vehicle networking (CAN, LIN-SBC, FlexRay)

***Impact*:** Secured multiple **long-term automotive design wins** and €15M in revenue by aligning customer technical requirements with commercial strategy across APAC Tier-1 accounts.

**Qimonda AG / Infineon Technologies AG**, Munich, Germany
**Senior IC Physical Designer – DRAM (DDR2/DDR3) & Mixed-Signal** | 2004.09 – 2009.07

• Led **full-custom physical design and sign-off** for **DDR2/DDR3 DRAM and mixed-signal products**, covering **DRC/LVS compliance** and tape-out readiness

• Executed **analog, mixed-signal, and power layout** across **90nm → 45nm CMOS nodes**, ensuring manufacturability, yield optimization, and device-matching precision

• Performed **digital P&R (ICC2)**, parasitic extraction, and **IR-drop / EM / antenna checks**, supporting robust timing and reliability sign-off

• Improved **design-cycle efficiency** by integrating digital blocks through **PCell-based methodologies and Virtuoso XL**, reducing manual layout effort

• Authored **technical guidelines** and contributed to **global analog layout methodologies (Leading global teams)**, enabling consistency and reuse across design teams

***Impact*:** Delivered **tape-out-ready DDR memory and mixed-signal silicon on schedule** while improving layout robustness, yield, and design-cycle efficiency across multiple technology nodes.

**Integrated Silicon Solution Inc. (ISSI)**, Hsinchu, Taiwan
**Senior IC Design Engineer** | 2004.01 – 2004.07

• Executed **mask revisions and layout optimization** for a **256Mb LP-SDRAM** product, covering RTL-to-GDS implementation and verification

• Supported **manufacturability improvements and sign-off quality**, ensuring alignment with **TSMC PRRM** requirements

***Impact*:** Enabled tape-out-ready LP-SDRAM design with improved verification robustness and manufacturability, reducing risk during foundry sign-off.

**SK-Hynix Semiconductor**, Icheon, South Korea
**Senior IC Design Engineer – DRAM Circuit & Physical Design** | 1996.02 – 2003.12

• Led **DRAM and SRAM circuit design and chip architecture definition**, covering high-speed clocks, sense amplifiers, power management, I/O, refresh, and control logic, with full-chip simulation and **JEDEC-compliant timing sign-off**

• Executed **HSPICE/HSIM simulations**, first-silicon debug, failure analysis, and **timing closure**, supporting reliable transition from design to volume production

• Coordinated **physical design teams** through floor-planning, tape-out, and full-chip sign-off, ensuring alignment across circuit, layout, and manufacturing interfaces

• Designed and verified **critical layout blocks** (I/O, ESD/latch-up protection, core arrays, power routing), performing **RC extraction, IR-drop, DRC/LVS/ERC/OPC sign-off**, and implementing **dummy-fill and CMP-aware optimizations** to improve wafer yield

• Led development of **design automation and P&R flows**, writing **Hercules and Assura rule decks** and supporting post-layout **SI and static timing analysis sign-off** using StarRC

***Impact*:** Supported multiple **high-volume DRAM product launches** by integrating circuit design, physical implementation, and automation flows, improving yield, sign-off robustness, and scalability in production.

## EDUACTION

**Bachelor of Science, Electronics Engineering**
University of Ulsan, South Korea (1989.03 – 1996.02)
Completed 29 months of mandatory **military service** with the Republic of Korea Army Infantry while pursuing degree studies (1991.01 – 1993.06)

**German Language Training (Professional Integration Track)**
Completed a series of certified German language programs supporting professional integration, technical communication, and customer-facing responsibilities in Germany:

• **B2** Level (2013.12–2014.05), CBZ München **| Berlitz Level 4** (2010.11–2011.04), Berlitz Dortmund **| B1** Level (2009.08–2009.12), Münchener Volkshochschule

**Japanese Language Course** in Dortmund (2010.02~ 2011.05), in KOR (1996.03~ 1996.08)

**Additional Training:**
• Advanced IC Physical Design & ICC P&R (Synopsys, Munich) (2018.03)
• Calibre SVRF / PERC / OPC Training (Siemens EDA/Mentor, Munich) (2014.09), and Trainer
• Microcontroller with infrared optical sensor (ELMOS, Karlsruhe) (2010.06 & 2011.09)

## Interests & Hobbies

• Machine Learning/AI, cloud-based EDA innovation, and European historical studies

• Long-distance running, hiking, cycling to support a balanced and healthy daily routine

**TECHNICAL HIGHLIGHTS** (Selected – Supporting Application & Customer Engagement)

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**Foundry Technology Coverage**

Practical exposure to advanced semiconductor process nodes **(≈45nm to 3nm-class)** across **major foundries** including TSMC, GlobalFoundries, Intel, and STMicroelectronics
**TSMC** (N28, N16, N7, N3E), **GlobalFoundries** (45nm, 22nm, 14nm), **Intel Foundry** (i1278, i1276, i1226), **STMicroelectronics** (45nm, 40nm, 28nm), **Samsung Foundry** (S16N, S14N)

**Manufacturing & Mask Data Preparation**
• Hands-on **lithography simulation**, SRAF / RET evaluation, **OPC**, Multi-patterning strategies
• End-to-end **mask data preparation** pipelines, sign-off-level expertise in **FinFET,** spanning **MEMS, optical, and CMOS** technologies

**CRM & Enterprise Systems**
• Salesforce • SAP CRM • JIRA
**Data & Markup Formats**
• JSON • HTML • XML • CSV
Design Data & Configuration Management
• Git • GitHub • Bitbucket • Visual Studio Code
**Programming & Automation**
• Python • Tcl • Perl • awk • Shell scripts (bash/csh) • Java • C++
**Operating Systems**
• High-performance computing (AWS cloud-enabled) • UNIX/Linux(RHEL, SLES) • Windows

**Selected EDA & Semiconductor Tools**
**Analog / Mixed-Signal Circuit Design & Simulation (TCAD)**
• HSPICE, Spectre, FastSpice (HSIM / NanoSim), Oscilloscope
**Physical Design, Verification & Full-Chip Sign-Off**
• Cadence Virtuoso XL, SKILL Pcell, Assura, Pegasus and Innovus, Klayout
• Synopsys ICC2, StarRC, PrimeTime, STA, IC Validation, Hercules (DRC / LVS / ERC / FILL)

**Siemens EDA / Mentor Calibre – Deep Expertise**
• Model/Rule-based OPC calibration, OPCVerify, OPCPro, lithography processes simulation SRAF Analyze, Resolution Enhancement Techniques (RET), Mask MEBES, Litho ModelFlow LithoView, multi-patterning, Workbench, DFM & Yield Analysis, PERC (ESD, latch-up)
• Smart-Fill/ECO-Fill, antenna, pattern matching, auto-waivers, FastXOR, RealTime

**Advanced debug & integration:** Photonic DRC (**curvilinear geometries**), 2.5D/3D IC
• Chiplet & **3D stack**, Xpedition (IC package), GUI, DESIGNrev/Workbench, Tanner, MTFLEX
• **SVRF, TCL/TVF,** Parasitic Extraction, xACT, mPower, DBDIFF, and database automation

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